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10/618,404	07/11/2003	Steven P. Young	X-1392 US	5533

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EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/618,404	YOUNG, STEVEN P.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-7 and 21-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 21-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Amendment filed 4-7-2005.

Claim Objections

Claim 21 is objected to because of the following informalities:

"integrated circuit" on lines 6 and 7 appears to be --integrated circuit die--

respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Seefeldt et al. (US PAT No. 4,978,633).

Regarding claim 1, Fig. 2 of Seefeldt et al. teaches an integrated circuit (IC) having programmable interconnections (41; col. 2, lines 5-18), comprising: a first plurality of regions (31, 32), each region having a programmable circuit with a programmable function (col. 2, lines 21-29); and a second plurality of areas (6x6 array include 6 columns and 6 rows) of the IC, wherein each area of the second plurality extends from one edge of the IC to an opposing edge of the IC (a single 6x6 die is separated by scribe lines from a wafer, which creates 6 columns extending from two opposing edges as shown in Fig. 2), and wherein each area of the second plurality

comprises predetermined regions of the first plurality (each column has 31 and 32), wherein the predetermined regions in an area are in a column area substantially fill the area (each column is filled with 31 and 32) and wherein each of the predetermined regions in a first area comprises programmable circuits which are substantially identical and have a first function (first column from the left has 4 I/O super cell and 2 gate supercells such that identical I/O supercells are substantially filled the first column) and each of the predetermined regions in a second area comprises programmable circuits which are substantially identical and have a second function (first column from the right has 4 I/O super cell and 2 gate supercells such that identical I/O supercells are substantially filled the first column from the right).

Regarding claim 2, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 further comprising a third area of the second plurality of areas wherein every predetermined region in the predetermined regions in the third area has a circuit of only one circuit type (the second columns from the left and right edge has only GATE which is super logic function cell), the circuit type selected from a group consisting of Configurable Logic Block (CLBs), Multi-Giga Bit Transceivers (MGTs), Block Random Access Memories IBRAMs), Digital Signal Processor (DSP) circuits, Multipliers, and Input/output Blocks (IOBs).

Regarding claim 3, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 where an area of second plurality has predetermined regions comprising Multi-Giga Bit transceiver circuit (transceiver circuit in Fig. 3 handling input and output).

Regarding claim 4, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 1 further comprising a heterogeneous column area of the IC, the heterogeneous area of the second plurality of areas of the IC, the heterogeneous area having regions with programmable circuits that are of different circuit types (I/O or GATE).

Regarding claim 5, Fig. 2 of Seefeldt et al. teaches a die having an integrated circuit, comprising: a first set of regions (regions having I/O and Gate), each region in the first set having an Input/Output circuit (Fig. 3 shows I/O circuit), a second set of regions (regions having GATE supercells), each region in the second set having a circuit with a programmable logic function (supercell is configurable to perform a signal processing operation; ABSTRACT); a third set of columns (set of columns in Fig. 2), wherein a top of each column of the third set is positioned at a top side of the die and a bottom of each column of the third set is positioned at a bottom side of the die IC (a single 6x6 die is separated by scribe lines from a wafer, which creates 6 columns extending from two opposing edges, i.e. top and bottom sides, as shown in Fig. 2), a first column of the third set, where each region of the first column consisting essentially of regions from the first set (left-most column in Fig. 2 is a column essential of I/O supercells and GATE), and a second column of the third set (column right next to the

left-most column is a column essentially of super gate cell) consisting essentially of regions from the second set, wherein the second column is interposed between the first column and a nearest side edge of the die (the second column from the left is positioned between the left-most column, i.e. nearest side edge of the die, and the right column)

Regarding claim 6, Fig. 2 of Seefeldt et al. teaches the die of claim 5 wherein an Input/Output circuit comprises a Multi-Giga Bit Transceiver or an input/output block or a combination thereof (Fig. 3 discloses an input/output circuit).

Regarding claim 7, Fig. 2 of Seedfeldt et al. teaches the die of claim 5 further comprising a third column of the third set positioned at a center line of the die, the third set comprising assorted tiles (the third column and the fourth column from the left side is positioned at a center line with I/O supercells and GATE supercells).

Regarding claim 32, Fig. 2 of Seedfeldt et al. teaches an integrated circuit consisting essentially of tiles (I/O supercells and Gate supercells), the integrated circuit comprising an input/output block tile having four sides (I/O) and in a column of input/output block tiles extending from a first end to a second end (third and fourth column extended from the top to bottom), where the input/output block tile is bounded on each of its four sides by another tile (I/O has four side bounded by I/O and Gate).

Claims 21-25 and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimizu et al. (US PAT No. 5,341,049).

Regarding claim 21, Fig. 1 of Shimizu et al. teaches a method, comprising: providing a plurality of configurable logic blocks in a first column (columns of 6A and I/O), the column extending from a first side of an integrated circuit die to a second side of the integrated circuit die (each column extends from top edge to bottom edge; col. 3, lines 37-68); and providing a plurality of Input/Output blocks in a second column, the second column extending from the first side of the integrated circuit to the second side of the integrated circuit (each column extends from top edge to bottom edge; col. 3, lines 37-68);

Regarding claim 22, Fig. 1 of Shimizu et al. teaches the method of Claim 21, further comprising: providing a first input/output block (I/O1) on a first side of the first column (the first column being the second 6A column from the left-most); and providing a second input/output block (I/O2) on a second side of the first column.

Regarding claim 23, Fig. 1 of Shimizu et al. teaches the method of Claim 22, wherein there is no input/output block disposed between the column of configurable logic blocks and the first side of the integrated circuit die (no I/O between the left-most column of 6A and the left-most edge).

Regarding claim 24, Fig. 1 of Shimizu et al. teaches the method of Claim 21, wherein the first column includes the plurality of configurable logic blocks as well as a plurality of clock distribution tiles (clocks distributed in 6A, col. 9, lines 11-33).

Regarding claim 25, Fig. 1 of Shimizu et al. teaches the method of Claim 21 wherein over ninety-five percent of the die area of the first column is occupied by configurable logic blocks (the left most column being the first column is filled with logic circuit cell 6A).

Regarding claim 30, Fig. 1 of Shimizu et al. teaches an integrated circuit comprising a plurality of configurable logic block tiles (6A) and a plurality of input/output block tiles (I/O1...I/O7) disposed in columns, each of the columns extending in a first direction (top to bottom), wherein no two input/output block tiles of the integrated circuit are disposed adjacent to one another to form a row that extends in a second direction perpendicular to the first direction (each column of I/Os are separated by 6A along left to right side).

Regarding claim 31, Fig. 1 of Shimizu et al. teaches the integrated circuit of Claim 30 where the integrated circuit comprises at least three columns of input/output block tiles (I/O1... I/O7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seefeldt et al..

Regarding claim 26, Fig. 2 of Seefeldt et al. teaches an integrated circuit comprising a column of input/output block tiles (third column from the left filled with 4 I/O cells and 2 Gate supercells) where the column of tiles occupies a die area and a first configurable logic block tile (second column from the left filled with Gate supercells) disposed on a first side of the column; and a second configurable logic block tile (fifth column form the left, filled with Gate supercells) disposed on a second side of the column opposite the first side where the I/O supercells and Gate supercells are dispersed in order to obtain better routability (col. 6, lines 12-23), but does not disclose the specific value of ratio of I/O supercells and Gate supercells being over ninety-five percent of the die area. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the specific value of ration being over 95% since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable value or ranges of an effective variable involves only routine skill in the art (see In re Boesch, 617 F2d 272, 205 USPQ 215(CCPA 1980) and In re Aller, 105 USPQ 233).

Regarding 27, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 26 where each of the input/output block tiles in the column has an identical layout (Fig. 3 shows topology for I/O supercells used in Fig. 2).

Regarding claim 28, Fig. 2 of Seefeldt et al. teaches the integrated circuit of claim 26 where the integrated circuit is a field programmable gate array (a gate array of supercells programmable, col. 3, lines 11-42).

Regarding claim 29, Fig. 2 of Seefeldt et al. teaches the integrated circuit of Claim 26, wherein the integrated circuit is disposed on a semiconductor die, the semiconductor die having a first side (top), a second side (bottom) opposite the first side, a third side (left), and a fourth side (right) opposite the third side, and wherein the column of input/output block tiles extends from the first side and to the second side (left-most column extends from the top to bottom), a first input/output block tile of the column (top I/O on the left-most column is adjacent to the top side) being disposed adjacent the first side of the die, a second input/output block tile of the column (bottom I/O on the left-most column is adjacent to the bottom side) being disposed adjacent the second side of the die.

Response to Arguments

Applicant's arguments with respect to claims 21 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 1 and 5, applicant argues that the geometry of the gate array is not fixed and the input/output and gate logic cells are intermingled rather than columns. The examiner notes that the size and geometry of the gate array is set based on applications, e.g. 6x6 or 3x3 by separating from wafer as discussed in col. 6, lines 56-57. One example is shown in Fig. 2 which has 6 columns and 6 rows of supercells where each column extends from top edge of a die to bottom edge of the die and each row extends from left edge of the die to left edge of the die. Regarding claim 26, applicant argues that "a column of input/output block tiles" would distinguish over Seefeldt. The examiner notes that Seefeldt discloses the intermingling of input/output supercells with gate supercells is based on the applications of the gate array circuit. Regarding claim 32, Seefeldt discloses all limitations as discussed above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

June 14, 2005